REMARKS

Claims 23-36 were pending when last examined. A complete listing of all claims is provided above.

Specification

According to the Examiner, "The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed."

Applicants respectfully traverse. The title of the present Application recites "Semiconductor Device Having Multi-Chip Package Structure." Each of the pending independent claims (i.e., Claims 23 and 30) recite in the respective preamble "semiconductor device having a multi-chip package structure." As such, the title of the invention is descriptive of the claimed invention.

Claim Rejections - 35 USC § 102

Claims 23-26 and 30-33 stand rejected under 35 U.S.C. 102(e) as being anticipated by Martinez et al. (U.S.P.N. 6,184,585). According to the Examiner, Martinez et al. discloses a "co-packaged MOS-gated device and control integrated circuit having all of the claimed subject matter" where "'a lead frame' is met by the lead frame 40," "'a first integrated circuit chip...of the first integrated circuit chip' is met by the first integrated chip Q2 attached to a top surface of the lead frame 40 by a conductive adhesive 42, wherein the first integrated circuit chip Q2 does not have a passivation layer on a top surface of the first integrated circuit chip Q2," and "'a second integrated circuit chip...by an insulation epoxy adhesive' is met by the second integrated circuit chip 16 directly attached to the top surface of the first integrated circuit chip Q2 by an insulation epoxy adhesive." Applicants respectfully traverse.

A passivation layer is formed in all metal-oxide-semiconductor field effect transistor (MOSFET) fabricating processes. This is clearly shown, for example, in

U.S.P.N. 6,404,025 entitled, "MOSFET power device manufactured with reduced number of masks by fabrication simplified processes," which shows a passivation layer 60 in Figure 1 and recites, "a passivation layer is required to prevent mobile ions from entering into the device." col. 2, lns. 3-4

In contrast, Applicants describe and claim a semiconductor device which includes an integrated circuit chip not having a passivation layer on its top surface. As stated in the specification of the present Application, "the first integrated circuit chip 15 may not have a passivation layer on its top surface; only a metallization layer may be formed on the top surface." See Specification, p. 4, lns 8-10. The present Application teaches that "the reliability of a power semiconductor device not having a passivation layer is significantly better than the reliability of a power semiconductor device having a passivation layer." See Specification at p. 8, lns 29-31. In addition to the improvement in reliability, the present Application teaches that "a power semiconductor device not having a passivation layer reduces manufacturing cost and simplifies manufacturing processes..." See Specification, p. 9, lns 1-5. There is no such similar teaching whatsoever in Martinez et al. Applicants respectfully submit that a passivation layer is present in integrated chip Q2 of Martinez et al.

Independent Claim 23 recites in pertinent part a "semiconductor device having a multi-chip package structure, the semiconductor device comprising...the first integrated circuit chip not having a passivation layer on a top surface of the first integrated circuit chip; and a second integrated circuit chip directly attached to the top surface of the first integrated circuit chip by an insulation epoxy adhesive." Martinez et al. does not describe or teach an integrated circuit chip not having a passivation layer on a top surface, and as such, Martinez et al. does not anticipate Applicant's claimed invention.

For at least the reasons discussed above, Applicant respectfully requests that the rejection of Claim 23 under 35 U.S.C. §102(3) be withdrawn and this claim be allowed.

Claims 24-26 depend from independent Claim 23 and include further limitations. Thus, for at least these reasons, Applicant respectfully requests the Examiner to withdraw

the rejection of Claims 24-26 under U.S.C. §102(e) and to allow these dependent claims as well.

Independent Claim 30 recites in pertinent part a "power semiconductor device having a multi-chip package structure, the power semiconductor device comprising...the switching device not having a passivation layer on a top surface of the switching device; and a driving device directly attached to the top surface of the switching device by an insulation epoxy adhesive." Again, Martinez et al. does not describe or teach an integrated circuit chip not having a passivation layer on a top surface, and as such, Martinez et al. does not anticipate Applicant's invention of Claim 30.

For at least the reasons discussed above, Applicant respectfully requests that the rejection of Claim 30 under 35 U.S.C. §102(e) be withdrawn and this claim be allowed.

Claims 31-33 depend from independent Claim 30 and include further limitations. Thus, for at least these reasons, Applicant respectfully requests the Examiner to withdraw the rejection of Claims 31-33 under U.S.C. §102(e) and to allow these dependent claims as well.

Claim Objections

Claims 27-29 and 34-36 are objected to as being dependent upon a rejected base claim. As discussed above, the independent claims (i.e., Claims 23 and 30) on which Claims 27-29 and 34-36 should be allowable. As such, Applicants respectfully request that the Examiner withdraw the rejection of these claims.

CONCLUSION

Applicants respectfully request that the pending claims be allowed and the case passed to issue. Should the Examiner wish to discuss the Application, it is requested that the Examiner contact the undersigned at (415) 772-1200.

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Respectfully submitted,

By: _____

Philip W. Woo
Attorney of Record
Reg. No. 39,880
PWW/rp

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SIDLEY AUSTIN BROWN & WOOD LLP
555 California Street, Suite 5000
San Francisco, CA 94104-1715
(415) 772-7200